AN ARBITER, A SYSTEM AND A METHOD FOR GENERATING

A PSEUDO-GRANT SIGNAL

BACKGROUND OF THE INVENTION

[0001] This U.S. nonprovisional application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 2003-33048 filed May 23, 2003, the contents of which are incorporated by reference in its entirety.

[0002] Arbitration mechanisms for improving bus bandwidth between at least one master and at least one target slave are known. The basic operation of such an arbitration includes a request, arbitration, grant, and data transfer.

[0003] When an arbiter grants bus ownership to a master, who requested access to a target slave, but the slave is unavailable to accommodate the data transfer, the result is a wasted grant of ownership, because the master must wait until the target slave is available for the data transfer. When the master accesses a target slave having long latency, the bandwidth is also degraded.

[0004] Figure 1 illustrates a conventional timing diagram, which illustrates a waiting time T. As shown in Figure 1, a first set of address information ADDR1-4 is supplied, followed by a first set of data DATA D1-D4. Subsequently, a second set of

address information ADDR5-8 is supplied, followed by a second set of data DATA

D5-D8.   As shown in Figure 1, the waiting time T is a delay between the availability

of data DATA D4 and D5.   This delay is undesirable.   Figure 2 illustrates a

desirable timing diagram where the waiting time T is eliminated.

[0005] Bank interleaving has been used as a conventional technique to divide a

memory into several banks, thereby permitting successive accesses to each bank.   In

bank interleaving, operations to each of the two banks is overlapped, for example,

data is accessed in one bank and pre-charged in another bank simultaneously, in order

to improve the bus bandwidth.

[0006] However, there are disadvantages with bank interleaving.   In particular, only

after the master receives bus ownership based on an arbitration, can the master drive

the valid address and control information.   Therefore, this information cannot be

used for arbitration because the information is generated after the arbitration.   As a

result, bandwidth improvements are limited.   Further, because the request to the

target slave can not be sent in advance, a waiting time delay, such as T described

above, still exists.

[0007] Other conventional devices include having a master generate a cycle type

signal at the same time as a request.   The cycle type signal indicates the specific

target resource (slave) to be accessed and whether the target is to be read or written.

Based on the cycle type signal and the related target resource information, the arbiter determines the priority of bus ownership. In this manner, a target slave retry cycle is avoided and bus bandwidth and overall system performance may be improved. However, additional pins are required to implement the cycle type signal and because the request to the target slave can not be sent in advance, the waiting time delay, such as T, still exists.

[0008] Figure 3 illustrates a conventional bus architecture, including masters 1-3, an arbiter 4, an SDRAM controller 5, and an SDRAM bank 6. Each master 1-3 requests bus access from the arbiter 4, via an HBUSREQN signal. The arbiter 4, which includes arbitration logic for selecting one of the masters 1-3, performs arbitration and grants access to the bus via an HGRANTN signal, which is supplied to the selected one among the masters 1-3. As shown in Figure 3, the HADDRN, HWRITEN, HBURSTN, HSIZEN, and HTRANN signals are each signals to drive a target slave. These signals are supplied from the masters 1-3 to the SDRAM controller 5 via one or more multiplexers (MUXs) 7-8. The MUXs 7-8 receive an HMASTER signal from the arbiter 4 and forward the selected HDDR, HWRITER, HBURSTR, HSIZER, and/or HTRANR to the SDRAM controller 5. MUX 7 receives an HWDATAN signal from each of the masters 1-3 and forwards the selected one among the HWDATAN signals as a BIWDATA signal to the SDRAM controller 5.

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The SDRAM controller 5, when ready, sends a BIREADYD signal to each of the masters 1-3. The SDRAM controller 5 also exchanges signals and data back and forth between the SDRAM 6.

[0009] Figure 4 illustrates a timing diagram of a conventional bus architecture. As indicated in Figure 4, a waiting time T exists between the transfer of the first data BODO-BOD3 and the second data B1D0-B1D3. This waiting time T reduces bus bandwidth efficiency and is caused by the fact the arbiter cannot request the target slave to prepare for data access prior to receiving the bus ownership through arbitration.

SUMMARY OF THE INVENTION

[0010] In exemplary embodiments, the present invention is directed to an arbiter in a system for generating a pseudo-grant signal to all requesting master units and for receiving transaction information from all requesting master units in response to the pseudo-grant signal.

[0011] In exemplary embodiments, the present invention is directed to a system which includes at least one master unit for generating a request, an arbiter for receiving the request from the at least one master unit and for generating a pseudo-grant signal in response to the request from the at least one master unit, the at least

one master unit supplying target information to the arbiter in response to the pseudo-grant signal, and at least one slave unit preparing for data transfer in response to the target information supplied by the at least one master unit.

[0012] In exemplary embodiments, the present invention is directed to a method of performing arbitration in a system, which includes generating a pseudo-grant signal in response to a request, and receiving target information in response to the pseudo-grant signal.

[0013] In exemplary embodiments, the present invention is directed to a method of performing arbitration in a system, which includes generating a request, receiving the request and generating a pseudo-grant signal in response to the request, supplying target information in response to the pseudo-grant signal, and preparing for data transfer in response to the target information.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The present invention will become more fully understood from the detailed description given below and the accompanying drawings, which are given for purposes of illustration only, and thus do not limit the invention.

[0015] Figure 1 illustrates a conventional timing diagram, which illustrates a waiting time T.

[0016] Figure 2 illustrates a desirable timing diagram where the waiting time T is eliminated.

[0017] Figure 3 illustrates a conventional bus architecture.

[0018] Figure 4 illustrates a timing diagram of a conventional bus architecture.

[0019] Figure 5 illustrates a bus arbitration structure in accordance with an exemplary embodiment of the present invention.

[0020] Figure 6 illustrates a timing diagram in accordance with an exemplary embodiment of the present invention.

[0021] Figure 7 illustrates a more detailed bus architecture of Figure 5 in accordance with an exemplary embodiment of the present invention.

[0022] Figure 8 illustrates another exemplary detailed architecture of the general bus arbitration scheme illustrated in Figure 5.

[0023] Figure 9 illustrates an exemplary timing diagram in accordance with the present invention.

[0024] Figure 10 illustrates the master interface illustrated in Figures 7 or 8 in accordance with an exemplary embodiment of the present invention.

[0025] Figure 11 illustrates a flow chart of a first stage of a method in accordance with an exemplary embodiment of the present invention.

[0026] Figure 12 illustrates a flow chart of a second stage of a method in accordance

with an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0027] Figure 5 illustrates a bus arbitration structure in accordance with an exemplary embodiment of the present invention. As illustrated in Figure 5, the bus arbitration structure includes N master units 110, 120, 130 where N is greater than or equal to one, an arbiter 140, and M slave units 150, 160, 170 where M is greater than one and not necessarily equal to N. In operation, each master unit 110, 120, 130 sends a request HBUSREQN to the arbiter 140. The HBUSREQ signal is a request signal to access a target slave, for example, slaves 150, 160, or 170. The arbiter 140 provides a pseudo grant signal HGRANT to each of the N requesting master units 110, 120, 130. The HGRANT signal is a signal to grant bus ownership to a master. Each of the N master units 110, 120, 130 then provides target information to the arbiter 140 for the arbiter 140 to perform arbitration. In the exemplary embodiment illustrated in Figure 5, the target information is signal HADDRN. The arbiter 140 performs arbitration and indicates data transfer is ready to occur by providing each master 110, 120 with a ready signal, HREADYN.

[0028] When two or more masters 110, 120, 130 request access to a bus, the HBUSREQN signals are asserted. In an exemplary embodiment of the present

invention, in such a situation, the arbiter 140 grants a "fake" or "pseudo" ownership to all of the requesting masters 110, 120, 130 by returning an HGRANTN signal prior to arbitration. The masters 110, 120, 130 receiving bus ownership, drive the desired information regarding the target slave (for example, HADDRN). The arbiter 140 utilizes this information and associated target slave information in order to perform the act of arbitration. After arbitration and checking the bus availability, the arbiter 140 sends the active HREADY signal to the selected master to indicate which actually has bus ownership.

[0029] Conventionally, an HGRANT signal is granted after arbitration. In exemplary embodiments of the present invention, the HGRANT signal is granted after a request, but prior to arbitration, as discussed above.

[0030] Figure 6 illustrates an exemplary timing diagram of the present invention. As illustrated in Figure 6, the HGRANT1 signal is triggered to high in response to the HBUSREQ1 signal. Further, HADDR1 signal is generated in response to a transition to high of HGRANT1 signal and is synchronized with HCLK. Similarly, the HGRANT2 signal is triggered to high in response to the HBUSREQ2 signal. Further, the HADDR2 signal is generated in response to a transition to high of HGRANT2 signal and is synchronized with HCLK. As also shown in Figure 6, the data information HRDATA, including DATA1 is generated in response to the

HREADY1 signal and the data, in particular DATA5, is generated in response to the HREADY2. As shown in Figure 6, the arbiter 140 receives the HADDR2 signal from the master 110, 120, 130 earlier in the exemplary embodiment of the present invention, thereby reducing a timing delay.

[0031] In Figure 7 and/or 8, the HADDR, HBURST, HWRITE signals are each signals to drive the target slave. The BIREQD signal is a signal to request a target slave to prepare for data access. The BIADDR, BIBA, BIRCONT, BICCONT are all signals including information to control a target slave. The BICONFIRMD signal is an acknowledgement (ACK) signal to the BIREQD signal. The NDCAS, NRAS, NCAS, NDWE signals are command signals to access a target slave or in other exemplary embodiments, a particular, specific memory bank. The BA signal is a bank address signal, the BIREADYD signal is a signal that is triggered to be activated when a target slave is ready to accommodate a data transfer. The HREADYN signal is a signal to indicate that a particular master now has the bus ownership for a data transfer from/to a target slave.

[0032] Figure 7 illustrates a more detailed bus architecture of Figure 5 in accordance with an exemplary embodiment of the present invention. As illustrated in Figure 7, the arbiter 550 includes a master interface 552 and a slave controller interface 554. The master interface 552 interacts with the N master units 510, 520, 530 and the slave

controller interface 554 interacts with M slave controllers 571, 572, 573. The M

slaver controllers 721, 572, 573 control one or more slave units 541, 542, 543.

[0033] As indicated in Figure 7, each master unit 510, 520, 530 provides an

HBUSREQ signal to the arbiter 550. The arbiter 550 generates an HGRANT signal

to each of the master units. Each of the master units then provides an HADDR

signal, an HBURST signal, and/or an HWRITE signal to the arbiter 550.

[0034] Each of the master units 510, 520, 530 supplies an HWDATAn signal to a

multiplexer (MUX) 560 and a selected one of HWDATAn as BIWDATA is supplied

to the slave controllers 571, 572, 573. The slave controllers 571, 572, 573 transfer

data to and from the slave units 541, 542, 543. The slave controllers 571, 572, 573

also provide a   BIRDATAn signal to a multiplexer(MUX) 580 and a selected one of

BIRDATAn as BIRDATA is supplied to the master units 510, 520, 530. .

[0035] Figure 8 illustrates another exemplary detailed architecture of the general bus

arbitration scheme illustrated in Figure 5. As shown in Figure 8, the arbiter 250

includes a master interface 252 and an SDRAM controller interface 254. The master

interface 252 interacts with the master units 210, 220, 230 and multiplexer 260, in

much the same way as described above in conjunction with Figure 7. The SDRAM

controller interface 254 supplies BIREQD, BIADDR, BIBA, BIBE, BIRCONT, and

BICCONT signals to an SDRAM controller 270 and receives a BIREADYD, and

BICONFIRMD signal from the SDRAM controller 270. The SDRAM controller receives BIWDATA from the selected one of the master units 210, 220, 230 of the MUX 260 and provides BIRDATA to the selected one of the master units 210, 220, 230. The SDRAM controller 270 supplies NDCS, NRAS, NCAS, NDWE, BA, and ADDR signals to an SDRAM 240 and receives data back from the SDRAM 240. In an exemplary embodiment, the SDRAM 240 includes one or more memory banks, identified as elements 241, 242, 243, and 244.

[0036] Figure 9 illustrates an exemplary timing diagram in accordance with the present invention. As illustrated in Figure 9, the master is able to send information early because the arbiter permits early sending via the pseudo grant signal. The arbiter may request the slave to prepare for data transfer via the RAS1 and CAS1 signals because the arbiter can receive the information of the target slave early

[0037] Figure 10 illustrates an exemplary embodiment of the master interface illustrated in Figures 7 or 8. As shown in Figure 10, the master interface 252, 552, includes synchronizer units 1001, 1002, 1003, each of which receives an HBUSREQ signal from a master unit and outputs an HGRANT signal. The master interface 252, 552 further includes multiplexers (MUXs) 1005, 1006, 1008 which receive the BIREADYD signal indicating that the target slaves are ready to transmit data and output one or more HREADY signals. As indicated in Figure 10, the master

interface 252, 552 need not include any arbitration logic.

[0038] Figure 11 illustrates a flow chart in accordance with an exemplary embodiment of the present invention. As shown at step 310, the arbiter determines whether at least one master is requesting bus access. If not, the arbiter stays in a holding loop. If yes, the arbiter sends an HGRANT signal to all requesting master units at step S320. At step S330, the arbiter receives drive information from all requesting master units. At step 340, based on the bus drive information and the status information of the target slave, a particular master is selected by the arbiter.

[0039] At step S350, to reduce latencies associated with the target slave regardless of bus availability, the arbiter request the target slave accessed by the selected master to prepare for data transfer. At S360, the slave controller sends the command signal to the target slave. The flow chart illustrated in Figure 11 may be considered a first stage of the exemplary method of the present invention.

[0040] Figure 12 illustrates a second stage, where the arbiter determines at step 410, whether any target slaves have finished preparing the data transfer. If not, the arbiter stays in the holding loop. If yes, the arbiter determines at step 420 whether the bus is available. If the bus is not available, the arbiter stays in a holding loop. If the bus is available, the arbiter selects one of the requesting masters attempting to access target slaves which have finished preparing the data transfer, at step 430. At step

440, data is transferred between the selected bus master and the associated target slave and the process repeats.

[0041] As described above, exemplary embodiments of the present invention modify the order of arbitration signals from the conventional order. In particular, in exemplary embodiments, the pseudo grant signal precedes the arbitration. Further, in exemplary embodiments, the information transfer precedes the arbitration so that the information contained in the data transfer may be used in the arbitration decision. Exemplary embodiments of the present invention reduce or eliminate a waiting time T and/or enable better arbitration decisions due the additional information available.

[0042] Although the exemplary embodiments of the present invention describe specific controller interfaces and memories, any other interfaces and/or memories could be utilized, as would be known to one of ordinary skill in the art. Still further, although the exemplary embodiments of the present invention describe a particular bus contention, the teachings of the present invention could also used to resolve any other bus contention, or any other resource contention, as would be known to one of ordinary skill in the art

[0043] The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to

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one skilled in the art are intended to be included within the scope of the following

claims.